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Joseph R. Tufts, Phillip J. MacQueen, Gary J. Hill, "Hobby-Eberly Telescope: LRS-J HAWAII-1 detector electronics," Proc. SPIE 4841, Instrument Design and Performance for Optical/Infrared Ground-based Telescopes, (7 March 2003); doi: 10.1117/12.461739

Event: Astronomical Telescopes and Instrumentation, 2002, Waikoloa, Hawai'i, United States

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ABSTRACT

The first second-generation instrument for the Hobby-Eberly telescope is a novel J band camera (LRS-J) which mates to the existing low resolution spectrograph (LRS). This camera uses the existing LRS longslit and mutltiobject units as well as the LRS five element collimator but uses its own J optimized volume holographic grisms, $f/1$ cryogenically cooled camera, and readout electronics built around a Rockwell HAWAII-1 array.

We minimized the development time of the controller by reusing as much of the existing framework as possible. The modular design of the existing LRS CCD controller allows us to modify only the clock-driver and penthouse (pre-amplifier) modules. Furthermore, we were able to use existing multilayer circuit boards already fabricated for these two modules. Thus, the LRS-J controller required only the substitution of components on two modules and the design of a new header (dewar) board to fit the HAWAII-1 socket. With these modifications, based on its perfomance with CCDs, we predict a noise and crosstalk performance at the most competitive level.

Keywords: HAWAII, LRS-J, HET, Hobby-Eberly Telescope, IR, electronics, controller, array

1. INTRODUCTION

The Hobby-Eberly Telescope (HET), located at the University of Texas McDonald Observatory in the Davis mountains of West Texas, presently has two operational facility instruments. The first-generation instruments are a grism-based low resolution imaging spectrograph (LRS), a intermediate resolution optical/near-IR fiber-fed cross-dispersed echelle spectrograph (MRS/JCAM), and a fiber-fed cross dispersed high resolution spectrograph (HRS).

From the beginning, the LRS was designed with camera upgradability in mind. The LRS five element collimator is achromatic into the near-infrared (IR). Assuming a suitable detector could be found, it was determined that a scientifically useful spectrograph could be made to operate out to 1.35 μm (J-band) without the need for a completely cooled instrument.[1,2] The tight space and weight constraints of the HET top end require us to use a catadioptric optical design resulting in a detector located in the beam, but the camera is able to make use of the LRS's three modes: imaging, multiple slit-width longslit spectroscopy, and 13 slitlet multi-object spectroscopy without the need for a completely new spectrograph.

Given the folded optical design we selected a Rockwell Scientific HAWAII-1 device for the LRS-J near-IR extension. Relative to the optical CCD (a 3K $\times$ 1K Ford Aerospace device), the HAWAII-1 is smaller requiring a shorter focal length and therefore faster camera. LRS-J is an $f/1$ camera with a 170 mm clear aperture and its optical design is well described elsewhere in these proceedings.[3,4]

Our initial intention of purchasing an "off the shelf" controller for our HAWAII-1 was abandoned in favor of the vastly more appealing custom controller. Primarily for the experience, compatibility, and cost effectiveness, we have built a controller tightly based on the current McDonald Observatory V2 CCD controller. Because the use of the LRS CCD system and LRS-J are mutually exclusive, LRS-J reuses most of the existing modules, and has identical cabling to the CCD system. We have built only a customized clock driver module and penthouse module (housing preamplifiers and bias supplies) for LRS-J, but even these are built on circuit boards identical to those found in the standard V2 CCD controller. This extreme reuse of component modules has the additional benefit of minimizing controller specific software and the bugs associated with its development. By eliminating many of the time consuming and labor intensive steps of controller development, we have been able to focus more of our energy on understanding this new technology.

Instrument Design and Performance for Optical/Infrared Ground-based Telescopes,
Masanori Iye, Alan F. M. Moorwood, Editors, Proceedings of SPIE Vol. 4841 (2003)

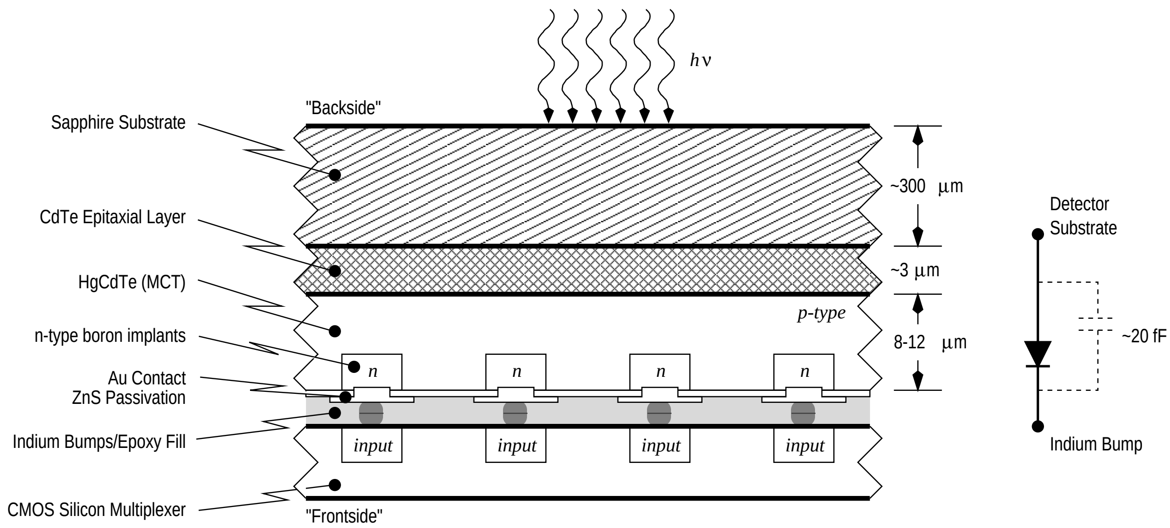


Figure 1. PACE-1 cross section.[11–14] The sapphire substrate is at an intermediate index of refraction which helps reduce the reflection from the CdTe epitaxial layer. PACE-1 photodiode orientation differs from newer MBE/DLPH detectors which use *p*-type implants in an *n*-type substrate. Successful optimization of the $f/1$ LRS-J optical system required us to account for the sapphire substrate thickness.

2. HYBRID INFRARED ARRAYS

LRS-J will use a HAWAII-1 device from Rockwell Scientific,[5] but we have designed the controller to allow detector upgrade to either a HAWAII-1R or HAWAII-2 type device. InSb arrays such as the Alladin arrays from Raytheon can be supported, but, due to the drastically different signal levels encountered in the Raytheon arrays, a dedicated clock driver module would need to be built.

Since its discovery in 1959 by Lawson, Nielsen, Putley and Young,[6] Mercury Cadmium Telluride (HgCdTe/MCT) has become one of the most well-studied semiconductor materials available, perhaps third only to Si and GaAs. HgCdTe is ideally suited to the prototype quantities required by near-IR astronomers since it is a *tunable* detector medium. That is, the band gap energy, E_g, of $Hg_{1-x}Cd_xTe$ depends only on mole fraction, x, and absolute temperature, T (the ratio of $[Hg+Cd]$ to Te typically remains near unity). Thus semi-prototype detectors can be fabricated with an approximate cutoff wavelength (in μm) computed as $\lambda_c \approx 1.24/E_g$, where E_g ranges from 0.0 – 1.605 eV.[6–8]

We have decided to concentrate our effort on Rockwell HgCdTe hybrid arrays[5, 9, 10] which, compared to available InSb arrays, are less-expensive, easier to control, and more closely matched to typical McDonald Observatory conditions. Rockwell has focused their IR detector development on fabrication of suitable HgCdTe photodiode active layers and on successfully mating them to CMOS silicon multiplexers. Compared to the development cost, there are very few large format IR detectors made, so given a format, Rockwell's approach allows customization without the need for a unique multiplexer design. We have found that slight modifications in the Rockwell standard specification cost about an additional $50K.

2.1. Rockwell Scientific NICMOS3, PICNIC, and HAWAII-1 detectors

At the detector layer, the NICMOS3, PICNIC, and HAWAII-1 detectors are all based on Rockwell's PACE-1 (Producible Altertative to CdTe for Epitaxy) process.[12, 14] This process, now over a decade old, was designed to address the high cost and low availability of suitable CdTe substrates needed for production of thin HgCdTe active layers. In the PACE-1 process a ~ 3 μm thick CdTe layer is deposited on a 0.3 mm thick sapphire substrate, an 8–12 μm *p*-type HgCdTe active layer is then grown on the CdTe interface layer, *n*-type junctions are then formed with boron ion implantation, and, finally, metal contacts and indium bumps are added (see Figure 1). Although the sapphire substrate is both cost effective and more closely matches the Si multiplexer CTE, the CMOS MUX still requires thinning in larger format arrays.[11, 12] LRS-J is not affected by the major disadvantage of the PACE-1 process: since sapphire loses transparency at around 5 μm there is a fundamental cutoff despite the flexibility of HgCdTe.

The PICNIC and HAWAII-1 arrays primarily represent a multiplexer upgrade with respect to the NICMOS-3 arrays (figure 2).[13] The HAWAII-1 multiplexer is simply a larger format (1024^2 vs. 256^2), smaller pixel (18.5 μm vs. 40 μm) PICNIC-like device. Though all three are still designed in a quadrant format, the newer arrays use a dual-edge-triggered shift register in both slow and fast dimensions, replace pixel reset with line reset, and combine the clear register signal into the line sync and frame sync signals. The decreased pixel size and line reset of the HAWAII-1 array is designed to decrease the array's read noise making it more suitable for low background applications such as spectroscopy. The LRS-J controller supports both the NICMOS3 multiplexer and HAWAII-1 multiplexer, as well as the newer HAWAII-1R/2 multiplexer. At present, we have only implemented the HAWAII-1 multiplexer firmware.

Of the three MOSFETs in each HAWAII-1 unit cell, one pMOS transistor acts as a source follower while the others act as gates. During a line reset, an active low RESETB pulse is NOR'ed with an inverted active high output from the row select register. This puts an analog-HIGH voltage on the nMOS reset transistor in all of a line's unit cells causing VRESET to charge the virtual capacitor created by the p-n junction in the HgCdTe active layer. Photons progressively discharge this reverse biased capacitor in a linear way during an integration. The active high READ pulse NAND'ed with the row select register puts a LOW voltage on the pMOS read gate transistor which dumps the pMOS source follower output to the column bus if the appropriate column is selected. Our working schematic (Figure 2) is developed from published versions,[15–17] published descriptions,[14, 18] and inferences from published NICMOS3 functional diagrams.[11, 19, 20]

2.2. Rockwell Scientific HAWAII-1R and HAWAII-2 detectors

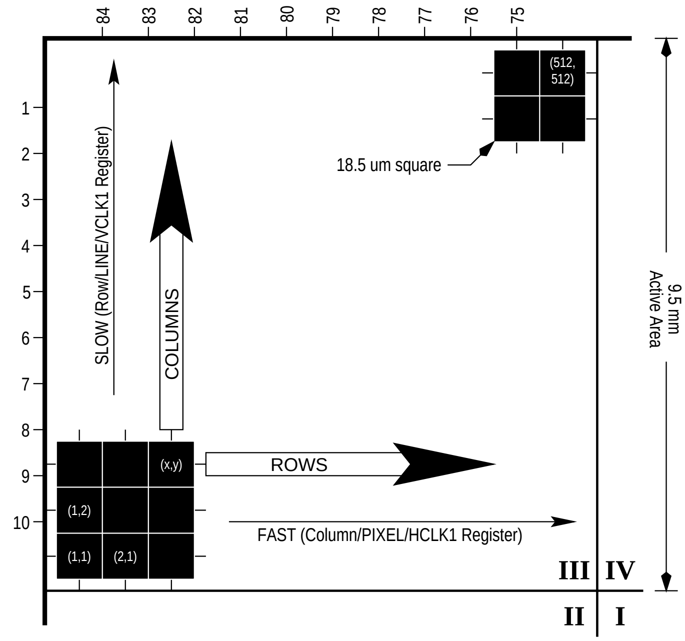
To astronomers the most frustrating annoyances of the NICMOS3, PICNIC, and original HAWAII devices, large shift register glow, high residual charge, low quantum efficiency, and slow maximum speed have all been addressed in the latest HAWAII-1R and HAWAII-2 devices (The HAWAII-1R has a 1014^2 imaging area in a 1024^2 18.0 μm format). Though this requires two external clocks (and their inversions), an attempt has been made to reduce the shift register glow by eliminating a CMOS inverter from each stage of the shift registers. Furthermore, the number of outputs is now user selectable to be one or eight per quadrant with either interlaced (alternating amplifier, shuffled) or striped (unshuffled) output available in the 8 amplifier mode. When necessary, this allows the system designer to choose between the fast/expensive 32 amplifier system and the slower/less expensive four amplifier mode. By design, the LRS-J controller, with only software modifications, can handle the four amplifier mode of either device. The LRS-J effort becomes a stepping stone towards a future 32 channel controller.

As an answer to the prototype quantities and one-off requirements of astronomers, Rockwell appears to have focused efforts on molecular beam epitaxy (MBE) for future manufacture of detector active layers.[21, 22] This technology essentially allows each array to be individually tuned to the design requirements of the purchaser. It appears that these active layers are intended to mate with the improved HAWAII-1R and HAWAII-2 multiplexers, despite the fact that prototype HAWAII-2 arrays were manufactured with PACE-1 active layers.[23]

We expect the MBE based arrays to demonstrate a more tunable quantum efficiency (QE) and decreased residual charge/dark current. The primary cause of the poor QE of the PACE-1 based arrays is high reflections from both the sapphire-air interface and the sapphire-CdTe interface. Rockwell found that there was little point in anti-reflection (AR) coating the sapphire substrate because the reflections resulting at the CdTe interface were equally strong. The residual charge, or, more correctly, the residual dark current increase[24, 25] which results after the exposure of a bright object and plagues all PACE-1 devices is believed to be due to the 8% lattice mismatch between the CdTe epitaxial layer and the HgCdTe active layer. Rockwell has addressed both of these issues with an MBE grown CdZnTe substrate. There is no lattice mismatch between this and the active layer, and the substrate can be reliably AR coated. The original motivation for the PACE-1 process, thermal mismatch between multiplexer and detector substrates is solved by thinning the multiplexer and mounting in a carrier which more-closely matches the CTE of CdZnTe. At the controller level, the MBE active layer differs from the PACE-1 active layer only in the sense that the MBE layer is built as arsenic doped *p*-type implants in an *n*-type HgCdTe active layer.[26, 27]

3. CONTROLLER

The LRS optical camera uses a McDonald V2 CCD controller. Since it is currently impossible to operate both an optical CCD and infrared array at any one time on the low resolution spectrograph (LRS), we have chosen to reuse as much of the existing controller hardware as possible. This scheme minimizes hardware handling, reduces cost, maintains in-house



Pin Name	Q1 pin	Q2 pin	Q3 pin	Q4 pin	Nominal
DSUB	34				0.0 V
CELLWELL	35				5.0 V
MUXSUB	48				0.0 V
VRESET	32	22	84	74	0.5 V
CELLDRAIN	33	23	83	73	0.0 V
BIASPOWER	39	27	79	69	5.0 V
BIASGATE	40	28	78	68	3.5 V
BUS	41	29	77	67	200 K to 5 V
SOURCE	42	30	76	66	10 K to 5 V
DRAIN	43	31	75	65	0.0 V
VSS	44	21	1	64	0.0 V
VDD	45	20	2	63	5.0 V
LOW	52	12	4	61	0.0 V
HIGH	53	11	3	62	5.0 V
LSYNC	36	24	82	72	0/5 V Act. Hi
PIXEL	38	26	80	70	0/5 V DE Trig.
LINE	46	19	8	57	0/5 V DE Trig
FSYNC	47	18	9	56	0/5 V Act. Hi
READ	49	15	7	58	0/5 V Act. Hi
RESETB	50	14	6	59	5/0 V Act. Lo
LINECHK	37	25	81	71	Output
FRMCHK	51	13	5	60	Output

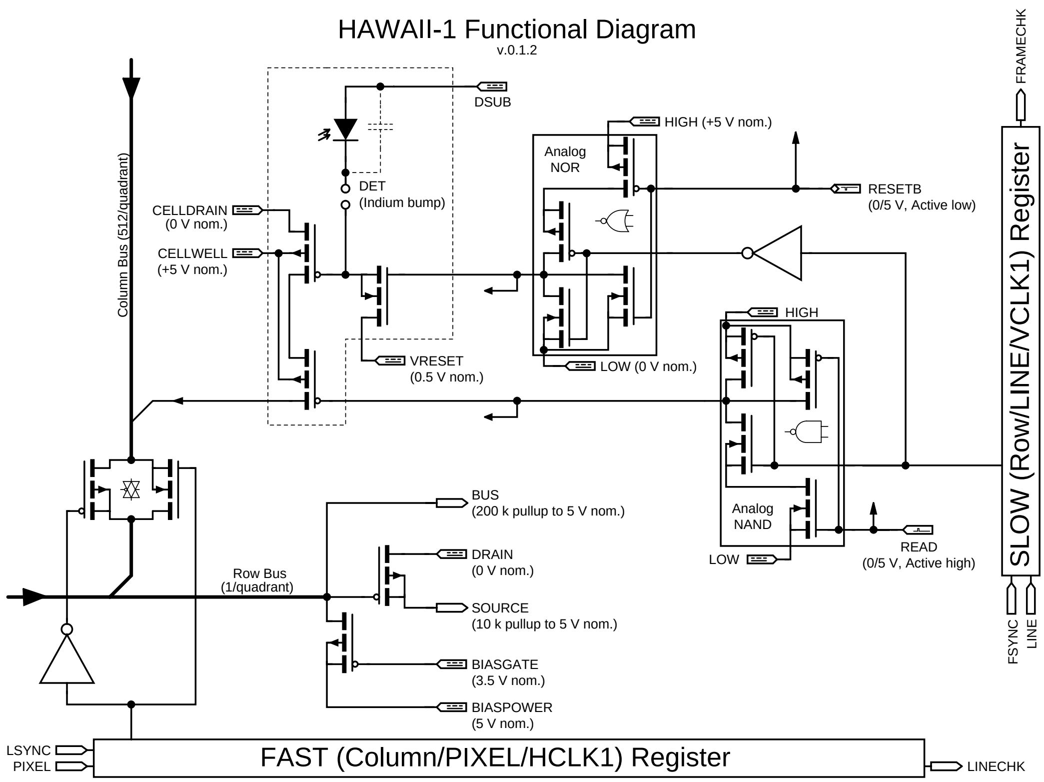


Figure 2. Rockwell HAWAII-1 pinout and functional diagram.[5, 15] Quadrant orientation in the HAWAII-1 is identical in all four quadrants, and the three pins DSUB, MUXSUB, and CELLWELL are common to all quadrants. The read/reset logic is replicated once for each row. Specification voltages are given, but we find a V_{DD} of 4.0 V reduces glow significantly. In typical operation we set CELLWELL, BIASPOWER, and HIGH to 5.0 V, and VRESET to 0.494 V.

ownership, decreases development time, and (we hope) increases performance in critical areas. Of the nine modules in the V2 controller, LRS-J will reuse the backplane, power supply, temperature controller, digital signal processor (DSP), shutter driver, and, initially, the two analog signal processors (ASP). The remaining two modules, the clock driver and penthouse (preamplifier), use printed circuit boards identical to those found in the CCD version of the controller. The LRS-J controller simply removes some unnecessary components, uses appropriate voltage references, and uses programmable bias ranges matched to the HAWAII devices.

3.1. LRS/LRS-J Common Modules

At the heart of both LRS and LRS-J detector controllers is a 40 MHz Motorola 56002 DSP. The DSP module is the system controller which communicates with seven other modules via a backplane. Additionally it communicates with an external PCI or SBUS SUN computer through a high speed (20 MB/s) fiber optic interface. The DSP module does not perform any DSP specific signal processing.

The LRS-J controller also uses the power supply, shutter control, and temperature control modules from the LRS controller. We believe the standard servo loop gain and time constants of the temperature controller will work with the thermal characteristics of the LRS-J cryostat. When used with the LRS CCD, SF1, the typical temperature error signal is on the order of 200 μK.

At present, the backplane limits the controller to two independent ASPs, each of which currently uses a single Analogic ADC5030 18-bit A/D converter. The LRS-J field aspect ratio is such that, using only two quadrants of an array, we lose only the most vignetted area of the 4 arc-minute HET field of view. We will operate the LRS ASPs in 16-bit mode by throwing away the two least significant bits (LSB). This resolution appropriately satisfies the needs of the HAWAII-1 device while simultaneously cutting the data volume in half by transmitting one 16-bit word per pixel (as opposed to two for 18-bit conversion). It also reuses existing ASP modules though we will eventually design and build a significantly faster dedicated ASP which will handle at least four channels.

Where HAWAII detectors have a source follower for each detector, it is not practical to use analog correlated double sampling as we do for CCD detectors. Though this halves the integration time required in the ASP module, it requires full digitization of both reset and signal levels. All data from both reset and signal frames will be transmitted to the controlling SUN workstation for processing. Multiple correlated sampling (Fowler sampling)[28, 29] is implemented by repeating the read array procedures *n* times at each end of the integration. Up the ramp sampling[30] is implemented by reading during an integration. Array clocking is highly modular allowing further customization and experimentation if necessary. All readout options, as well as full detector diagnostics are fully controllable from the familiar IRAF/ICE interface. This same command line interface is used to control the telescope allowing fully scripted observations.

3.2. Penthouse Module

All Rockwell arrays which we have discussed have a four-output mode, additionally the HAWAII-1R and HAWAII-2 devices have two 32-output modes. The LRS-J preamplifier circuitry (which, for historical reasons, we call the penthouse) is built on the same twelve layer circuit board used in a standard V2 CCD controller such as the LRS CCD controller. Each of the four preamplifier inputs is capacitively coupled to the array with a low leakage Component Research Co. 15 nF 50 V polystyrene capacitor. The preamplifier input source followers are matched-pair cascodes with tuned matched constant current sources. The capacitively coupled side of the pair drives the non-inverting input of an AD829, while the feedback loop of the 829 drives the inverting input through the other side of the matched pair (see Figure 3). In the LRS-J controller, the 829 drives an AD843 inverter which, in this application, acts as a triaxial line driver and a clamp preventing following stages in the ASP from saturating. We use Belden 88232 triax as a low-capacitance transmission medium from two of the four channels in the penthouse to the two independent ASPs.

Minor circuit modifications were necessary to adapt the programmable ranges of the bias supplies to those suitable for HAWAII devices (Figure 4). Non-inverting inputs of the AD847 op-amps were connected to ground through what was formerly a filter capacitor of an offsetting network. The AD847 power supplies were also switched from 0 V and 33 V to $\pm$15 V with some amount of board trickery. The 33 V power supply (formerly an LM317) was replaced with an LM1086IT-ADJ converting it to a +15 V regulator. Finally, over and under voltage protection circuitry (based on MAX976 comparators) needed modified voltage dividers. Careful modification of the penthouse circuit design allowed us to use an unpopulated CCD penthouse board for the LRS-J controller, and it eliminated the time consuming needs for both a custom penthouse board and custom programmed AMD MACH5 PLD to control the modified logic.

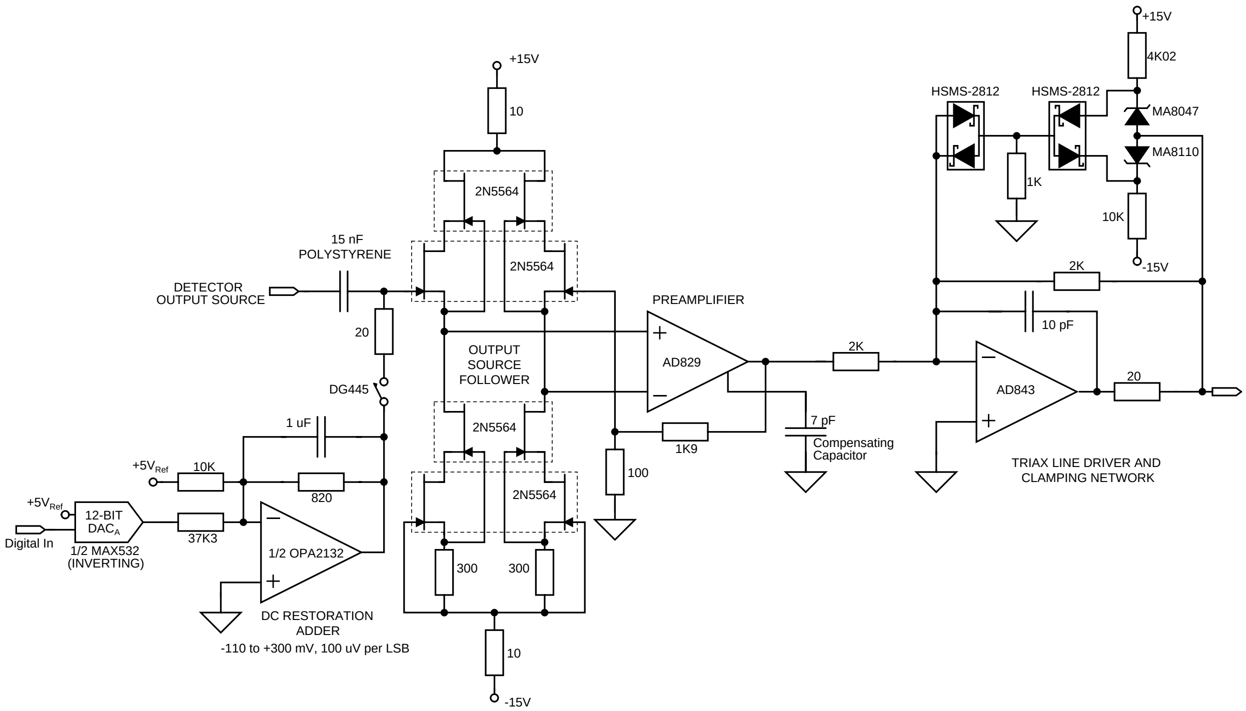


Figure 3. Simplified LRS-J preamplifier circuitry. For LRS-J the preamplifier gain of ~ 20 is entirely in the first stage AD829. Its gain is fully tunable to optimize the resolution of the 16-bit converter. We will sample detector read noise well at $1.5\ \bar{e}/\mathrm{ADU}$. Based on the controller's performance with Marconi CCDs, we hope to demonstrate reduced crosstalk relative to other groups.[31, 32] Note that certain bypass capacitors and other components are not shown, and the DC restoration switching circuitry is simplified.

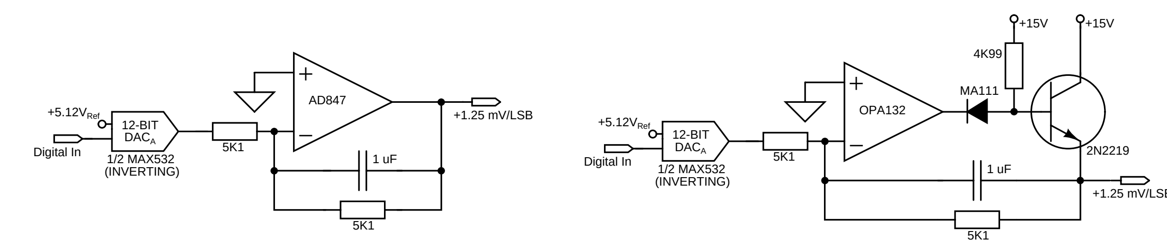


Figure 4. The modified bias supply circuitry for LRS-J. All HAWAII bias voltage levels are generated in the penthouse. 12-bit DACs set all levels with 1.25 mV precision. We use the AD847 as a buffer because of its unusual ability to drive infinite capacitance. The higher current V_{DD} and analog-HIGH inputs of the HAWAII-1 use an OPA132 with a 2N2219 emitter follower in the feedback loop.

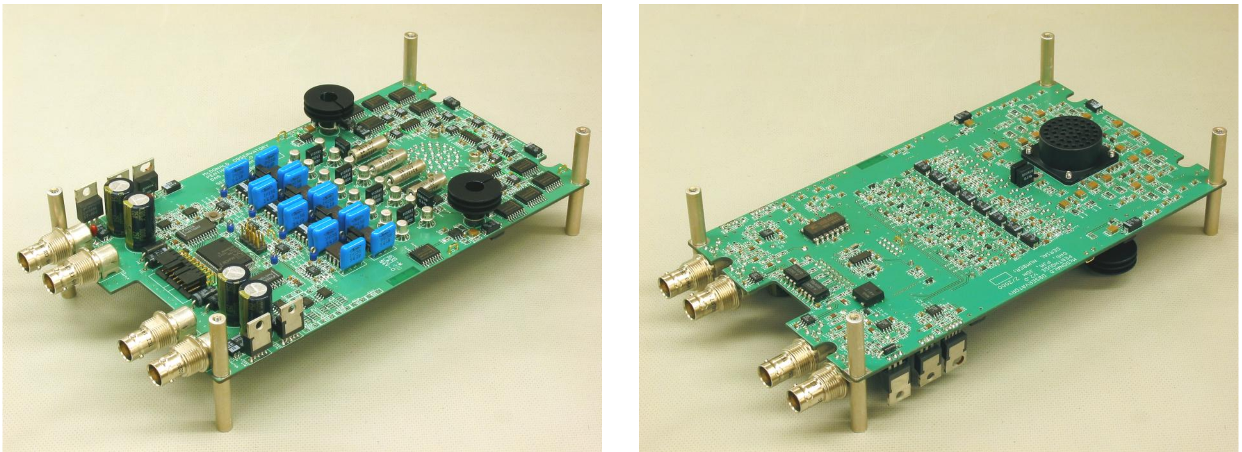


Figure 5. The completed LRS-J penthouse.

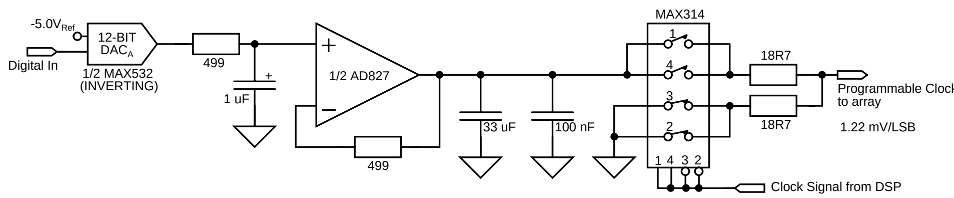


Figure 6. The modified circuitry for an LRS-J clock driver element. This unit cell is replicated 24 times on the LRS-J clock driver module. In this module the low level is fixed at ground, while the high level is programmable from 0–5 V in 1.22 mV increments. This circuit is capable of switching the array clock with 50 ns resolution.

3.3. Clock Driver

HAWAII-1 hybrid arrays, require six independent CMOS level clock signals per quadrant, but quadrants are typically operated in parallel and all four quadrants can be tied together. The LRS-J controller has 24 clocks in the clock driver and four in the penthouse. Though each of these has independently programmable levels, the DSP bus uses only nine control signals which are programmably multiplexed to the individual clock channels. We have mapped drivers to array pins in such a way that we can independently control the upper and lower halves of the HAWAII-1. This requires only 12 of the 28 available drivers, leaving the unused ones available for future control of a 1R or 2 multiplexer.

Figure 6 is a schematic of the circuit we use for each of the 24 drivers in the LRS-J clock driver module. The four clocks in the penthouse, which control RESETB on the HAWAII-1, are based on the AD827 instead of 847. The RESETB clocks are also 12-bit programmable from 0–5.12 V with 1.25 mV resolution. Otherwise the circuit is very similar to that shown.

3.4. Header/Dewar Interface Board

The LRS-J camera is an $f/1$ Maksutov design using an F2/SFL57 doublet, and fused silica primary. Its folded design puts the detector in the beam limiting some flexibility with design. The LRS-J field flattener is currently the largest obscuration, and, at 50 mm square, represents the largest allowable size for the header board. All cooled components must fit within this extremely tight space constraint.

We have purchased an IRLF25A from IR-Labs for prototyping and multiplexer experimentation. Since the silicon multiplexer is responsive to visible light, we will be able to fully test the controller with an uncooled system while simultaneously designing and procuring the final LRS-J header board. The IRLF25A uses a J230 with a 5K source resistor in an elementary source follower. Others[15] use the p-channel J270 or the TI TLC271. Any of these solutions

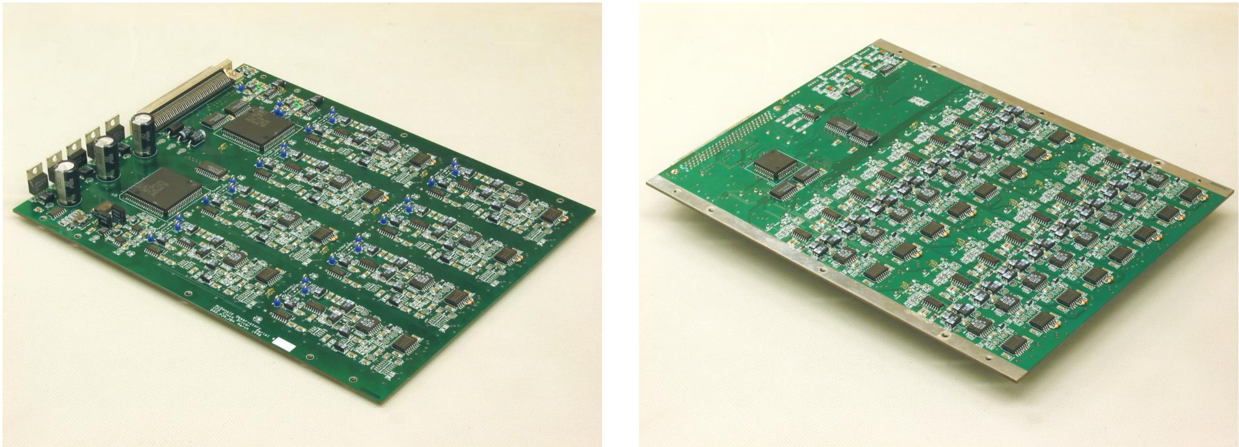


Figure 7. The completed LRS-J clock driver.

require exquisite temperature control to eliminate temperature dependent drifts. With the actual header board we would like to use a JFET cascode to improve linearity. The IRLF25A will aid us in that decision. It also affords us the opportunity to tune the controller in a warm environment.

4. SUMMARY

The LRS-J detector controller was assembled from existing CCD controller modules minimizing development effort. Furthermore, the only two custom modules were built on the same printed circuit boards as those found in the CCD controller. Most of the controlling software can be reused line for line. In a very short time frame we have built a custom controller capable of detector control for any of the Rockwell HgCdTe near-IR devices. LRS-J is now in the final stages of design, and we are fabricating many components. We fully expect to have a working multiplexer by the end of September and a working instrument within the next six months.

ACKNOWLEDGMENTS

The authors would like to thank Doug Edmonston for creative board level solutions and assembly of LRS-J modules, Gary Hansen for many years and help with system engineering and firmware programming. We would also like to thank Sam Odoms for the ICE interface programming and solutions in a pinch, and finally Jimmy Welborn for exquisite machining. This material is based upon work supported by the National Science Foundation under Grant No. 9987349.

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